

# United States Patent and Trademark Office

U

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
10/619,584	07/16/2003	Dong-Gyu Kim	SEC.310D3	7434
7590 05/04/2005			EXAMINER	
JONES & VOLENTINE, L.L.P.			TON, MINH TOAN T	
Suite 150 12200 Sunrise Valley Drive			ART UNIT	PAPER NUMBER
Reston, VA 20191			2871	
			DATE MAILED: 05/04/2009	5

Please find below and/or attached an Office communication concerning this application or proceeding.

· · · · · · · · · · · · · · · · · · ·	Application No.	Applicant(s)				
	10/619,584	KIM ET AL.				
Office Action Summary	Examiner	Art Unit				
	Toan Ton	2871				
The MAILING DATE of this communication Period for Reply	appears on the cover sheet wi	th the correspondence address				
A SHORTENED STATUTORY PERIOD FOR RE THE MAILING DATE OF THIS COMMUNICATIO  - Extensions of time may be available under the provisions of 37 CFI after SIX (6) MONTHS from the mailing date of this communication  - If the period for reply specified above is less than thirty (30) days, a  - If NO period for reply is specified above, the maximum statutory pe  - Failure to reply within the set or extended period for reply will, by st Any reply received by the Office later than three months after the mearned patent term adjustment. See 37 CFR 1.704(b).	NN. R 1.136(a). In no event, however, may a relation. I reply within the statutory minimum of thirt riod will apply and will expire SIX (6) MON atute, cause the application to become AB	eply be timely filed  y (30) days will be considered timely.  THS from the mailing date of this communication.  ANDONED (35 U.S.C. § 133).				
Status						
1) Responsive to communication(s) filed on $\underline{p}$	apers filed 01/31/05.					
2a)⊠ This action is <b>FINAL</b> . 2b)□ 1	This action is non-final.					
,	Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.					
Disposition of Claims						
4) ☐ Claim(s) is/are pending in the application 4a) Of the above claim(s) is/are with 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 36-41 is/are rejected. 7) ☐ Claim(s) is/are objected to. 8) ☐ Claim(s) are subject to restriction are	drawn from consideration.	•				
Application Papers						
9)☐ The specification is objected to by the Exam	niner.					
0)☐ The drawing(s) filed on is/are: a)☐ accepted or b)☐ objected to by the Examiner.						
Applicant may not request that any objection to	the drawing(s) be held in abeyan	ce. See 37 CFR 1.85(a).				
Replacement drawing sheet(s) including the cor						
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for fore a) All b) Some * c) None of:  1. Certified copies of the priority docum 2. Certified copies of the priority docum 3. Copies of the certified copies of the papplication from the International But  * See the attached detailed Office action for a	nents have been received. The sents have been received in Appropriate documents have been reau (PCT Rule 17.2(a)).	pplication No received in this National Stage				
* See the attached detailed Office action for a	ust of the certified copies not	eceivea.				
Attachment(s)		•				
1) ☑ Notice of References Cited (PTO-892) 2) ☑ Notice of Draftsperson's Patent Drawing Review (PTO-948)		ummary (PTO-413) )/Mail Date				
<ul> <li>3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB Paper No(s)/Mail Date</li> </ul>		formal Patent Application (PTO-152)				

Art Unit: 2871

## Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 36-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art (APA hereinafter, Figures 1-2) in view of Hiraishi et al (US 5831708) and Wakai et al (US 5327001).

APA discloses all except for the third signal line interposing the first and the second signal lines.

Basic/inherent elements such as a gate insulating layer, a semiconductor layer, a drain electrode, a source electrode, a protective layer having a contact hole exposing the drain electrode, a pixel electrode connected to the drain electrode through a contact hole are common and known in TFT (active matrix)-LCD devices. Wakai/Hiraishi discloses a conventional TFT-LCD device comprising basic/inherent elements such as a gate insulating layer, a semiconductor layer, a drain electrode, and a source electrode. Wakai discloses the LCD device comprising a protective layer having a contact hole exposing the drain electrode, a pixel electrode connected to the drain electrode through a contact hole for achieving advantages such as minimizing/preventing short circuit to the device. Therefore, it would have been at least obvious to one of ordinary skill in the art to employ basic/inherent elements such as a gate insulating layer, a semiconductor layer, a drain electrode, a source electrode, a protective layer having a

Art Unit: 2871

contact hole exposing the drain electrode, a pixel electrode connected to the drain electrode through a contact hole, as common and known in TFT (active matrix)-LCD devices, and also for achieving advantages such as minimizing/preventing short circuit to the device.

Hiraishi discloses (see at least col. 18, last paragraph to col. 19, first paragraph and an embodiment 7): in the conventional (common) device, an extra line is arranged outside of the display area, and a connection defect is repaired by connecting the disconnected section to the extra line with the irradiation of a laser. However, with this, there yields several disadvantages such as the number of lines which can be repaired is limited by the number of extra lines since providing a large number of extra lines is not preferred because this causes an increase in the non-display area. Hiraishi solves these disadvantages through forming the extra/repairing line (Applicant's third line) on the inside of the display area. Therefore, it would have been obvious to one of ordinary skill in the art to employ a third signal line interposing the first and second signal lines (formed on the inside of the display area) for avoiding disadvantages such as the number of lines which can be repaired is limited by the number of extra lines since providing a large number of extra lines is not preferred because this causes an increase in the non-display area. Hiraishi also discloses the connection lines passing between the adjacent gate lines and partly overlaps both the gate lines.

Forming the pixel electrode overlapping the bus lines is known in the art for yielding advantages such as large aperture (display area) ratio. Therefore, it would have been obvious to one of ordinary skill in the art to form the pixel electrode overlapping the bus lines (gate or/and data lines), as known in the art, for yielding advantages such as large aperture (display area) ratio.

Art Unit: 2871

## Response to Arguments

2. Applicant's arguments filed 01/31/05 have been fully considered but they are not persuasive.

Applicant contended that APA fails to disclose elements such as a gate insulating layer, a semiconductor layer, a drain electrode, a source electrode, a protective layer having a contact hole exposing the drain electrode, a pixel electrode connected to the drain electrode through a contact hole.

However, basic/inherent elements such as a gate insulating layer, a semiconductor layer, a drain electrode, and a source electrode are common and known in TFT (active matrix)-LCD devices (as at least disclosed by Wakai/Hiraishi). Further, Wakai discloses the LCD device comprising a protective layer having a contact hole exposing the drain electrode, a pixel electrode connected to the drain electrode through a contact hole for achieving advantages such as minimizing/preventing short circuit to the device. Therefore, it would have been at least obvious to one of ordinary skill in the art to employ basic/inherent elements such as a gate insulating layer, a semiconductor layer, a drain electrode, a source electrode, a protective layer having a contact hole exposing the drain electrode, a pixel electrode connected to the drain electrode through a contact hole, as common and known in TFT (active matrix)-LCD devices, and also for achieving advantages such minimizing/preventing short circuit to the device.

Art Unit: 2871

#### Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

#### **Contact Information**

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toan Ton whose telephone number is (571) 272-2303.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 2, 2005

